**Chaithanya Lakshmi Syba**

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**PROFESSIONAL SUMMARY**

Experienced Memory Layout Designer with 7+ years of industry expertise in eFuse, eFlash, MRAM memory designs and Python coding. Skilled in top-level and sub-level floorplan development, compiler code, memory block tiling, and layout creation for various components.

In my early career, I spent nearly 3+ years working as Assistant Professor at an esteemed university (JNTU). Now, I am seeking opportunities to contribute my knowledge and experience in a challenging environment.

**SKILLS**

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**Technologies worked on:** 12lpp, 22fdx, 28slpe, 28nm, 45nm, 40lp, 90nm, 130nm & 180 nm.

**Tools Exposure:** Cadence – Virtuoso, Assura, PVS, Voltus, Mentor Graphics – Pyxis, Calibre

**Coding:** Clojure, Verilog, C++

**Certification:** Certified on Full Custom Layout Design at RV VLSI Design Center, Bangalore.

**EXPERIENCE**

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**GLOBALFOUNDRIES BANGALORE, INDIA**

**MEMORY LAYOUT DESIGNER Jan 2020 to Date**

* Worked on eFuse, eFlash and MRAM memory designs.
* Responsibilities:
  + Develop the Top Level & Sub Level floorplan for compiler feasibility.
  + Develop the Clojure based compiler code to build Top level IP’s, and generate the CDL and GDS.
  + Optimizing memory layouts for complex chips using Python, Clojure, and C++ coding languages.
  + Tiling of memory blocks such as array, IO, Slice and control blocks.
  + Create the memory layouts such as bit cell, inverters, drivers, latch, mux, overlay’s, decoders for different drive strengths.
  + Take care of antenna & density violations and reliability issues
  + Apply Matching, shielding techniques for critical nets/signals/blocks.
  + Design of sense amplifier which is an analog block involving matching technique such as Common Centroid/ Interdigitation.
  + Handling blocks globally for power analysis/estimation.
  + Perform all verification checks like DRC, LVS, ERC, PEX, and EM for an IP at Chip/Cell/Blocks/Sub blocks.
  + Area saving without compromising the performance of the design.
  + Generated GDS, CDL, LEF and all verification reports for an IP for QA process.

**VARDHAMAN COLLEGE OF ENGINEERING HYDERABAD, INDIA**

**Assistant Professor** **April 2015 to Oct 2018**

* Responsibilities:
* Taught subjects including EDC, DLD, Basic VLSI Design, Verilog and Python Basics and Advanced CMOS VLSI Design to both undergraduate and postgraduate students.
* Conducted labs for EDC, PDC, VLSI, CMOS VLSI, and DDTV subjects for undergraduate and postgraduate students.
* Provided mentorship to students for their academic projects.
* Trained students in various domains such as Full Custom, Physical Design, and Verilog to prepare them for interviews.

**INTELLIMACH TECHNOLOGIES PVT LTD. HYDERABAD, INDIA** **Programmer**  **May 2013 to March 2015**

* Responsibilities:
  + Develop the Verilog HDL and C++ code to interface FPGA with microcontroller.
  + Netlist verification, BOM Generation
  + Handle the tasks of testing faults in modules after the production.

**EDUCATION \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**M.Tech – VLSI SYSTEM DESIGN HYDERABAD, INDIA**

J. N.T. U, Hyderabad Oct 2005 to April 2009

**B.Tech – ELECTRONICS & COMMUNICATION ENGINEERING HYDERABAD, INDIA**

J.N.T.U, Hyderabad Sep 2011 to Oct 2013

**ADDITIONAL INFORMATION**

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* Patent Award:
  + High voltage (3.6V) power switch at PAD with low voltage devices (1.8V) in Forming/Write modes in RRAM without SOA and low Area.
* Excellence Award:
* For excellent contribution across multiple areas by Chaitanya specifically On-Time project delivery, D&I, Team bonding activity lead, GF Bharat newsletter writer, GF Branding at external conferences like VLSID 2023.
* Spotlight Awards:
* Site award for excellent work for VLSID 2023 event which helped with GF India Branding.
* For hard work, smart work and commitment shown by Chaithanya in completing the design changes and solving complex EM issues for 45SPCLO eFuse IP release in very short time.
* For outstanding contribution towards GF team bonding activity and ISO training in 2Q-2022.
* Appreciation Awards:
* Received more than 15 appreciation awards in GlobalFoundries within 3+ years.
* Received International Women’s Day Award in 2021 Year

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